What is claimed is:

1. A magnetic memory device, comprising

a plurality of bit lines and a plurality of word lines, intersecting one another without being in contact to make up a matrix;

a plurality of memory cells provided at intersections of said plurality of bit lines and said plurality of word lines, including at least one magnetic tunnel junction;

a plurality of first switching means connected to first ends of said plurality of bit lines, being capable of switching the electrical connection between said first ends and a first power supply or a second power supply; and

a plurality of second switching means connected to second ends of said plurality of bit lines, being capable of switching the electrical connection between said second ends and said first power supply or said second power supply.

2. The magnetic memory device according to claim 1, wherein

said first switching means have first MOS transistors and second MOS transistors of the same conductivity type whose first main electrodes connected to said first ends of said plurality of bit lines, respectively, and second main electrodes connected to said first power supply and said second power supply, respectively, and

said second switching means have third MOS transistors and fourth MOS transistors of the same conductivity type whose first main electrodes connected to said second ends of said plurality of bit lines, respectively, and second main electrodes connected to said first power supply and said second power supply, respectively.

3. The magnetic memory device according to claim 1, wherein

said first switching means have first MOS transistors and second MOS transistors of different conductivity types whose first main electrodes connected to said first ends of said plurality of bit lines, respectively, and second main electrodes connected to said first power supply and said second power supply, respectively, and

said second switching means have third MOS transistors and fourth MOS transistors of different conductivity types whose first main electrodes connected to said second ends of said plurality of bit lines, respectively, and second main electrodes connected to said first power supply and said second power supply, respectively.

4. The magnetic memory device according to claim 3, further comprising:

fifth MOS transistors connected between said first main electrodes of said first and second MOS transistors, having the same conductivity type as that of said second MOS transistors; and

sixth MOS transistors connected between said first main electrodes of said third and fourth MOS transistors, having the same conductivity type as that of said fourth MOS transistors,

wherein control electrodes of said fifth and sixth MOS transistors are connected to a third power supply supplying a predetermined voltage which always brings an ON state.

5. A magnetic memory device, comprising:

a plurality of memory cell arrays consisting of

a plurality of bit lines and a plurality of word lines, intersecting one another without being in contact to make up a matrix, and

a plurality of memory cells provided at intersections of said plurality of bit lines

and said plurality of word lines, including at least one magnetic tunnel junction; and

at least one memory cell array group having

a plurality of main word lines provided across said plurality of memory cell arrays, and

a plurality of memory cell array selecting lines provided correspondingly to said plurality of memory cell arrays,

wherein said plurality of word lines are connected to outputs of first combined logic gates which are provided at intersections of said plurality of main word lines and said plurality of memory cell array selecting lines, respectively, and

inputs of said first combined logic gates are connected to one of said plurality of main word lines and one of said plurality of memory cell array selecting lines which intersect each other.

6. The magnetic memory device according to claim 5, wherein

said at least one memory cell array group includes a plurality of memory cell array groups,

said magnetic memory device further comprising:

a plurality of global word lines provided across said plurality of memory cell array groups; and

a plurality of memory cell array group selecting lines provided correspondingly to said plurality of memory cell array groups,

wherein said plurality of main word lines are connected to outputs of second combined logic gates which are provided at intersections of said plurality of global word lines and said plurality of memory cell array group selecting lines, respectively, and

inputs of said second combined logic gates are connected to one of said plurality

of global word lines and one of said plurality of memory cell array group selecting lines which intersect each other.

7. A magnetic memory device, comprising:

a plurality of memory cell arrays consisting of

a plurality of bit lines and a plurality of word lines, intersecting one another without being in contact to make up a matrix, and

a plurality of memory cells provided at intersections of said plurality of bit lines and said plurality of word lines, including at least one magnetic tunnel junction; and

at least one memory cell array group having

a plurality of main bit lines provided across said plurality of memory cell arrays, and

a plurality of memory cell array selecting lines provided correspondingly to said plurality of memory cell arrays,

wherein said plurality of bit lines are connected to outputs of first combined logic gates which are provided at intersections of said plurality of main bit lines and said plurality of memory cell array selecting lines, respectively, and

inputs of said first combined logic gates are connected to one of said plurality of main bit lines and one of said plurality of memory cell array selecting lines which intersect each other.

8. The magnetic memory device according to claim 7, wherein

said at least one memory cell array group includes a plurality of memory cell array groups,

said magnetic memory device further comprising:

a plurality of global bit lines provided across said plurality of memory cell array groups; and

a plurality of memory cell array group selecting lines provided correspondingly to said plurality of memory cell array groups,

wherein said plurality of main bit lines are connected to outputs of second combined logic gates which are provided at intersections of said plurality of global bit lines and said plurality of memory cell array group selecting lines, respectively, and

inputs of said second combined logic gates are connected to one of said plurality of global bit lines and one of said plurality of memory cell array group selecting lines which intersect each other.

9. A magnetic memory device, comprising:

a memory cell array consisting of

a plurality of bit lines and a plurality of word lines, intersecting one another without being in contact to make up a matrix, and

a plurality of memory cells provided at intersections of said plurality of bit lines and said plurality of word lines, including at least one magnetic tunnel junction; and

an inductor,

wherein said at least one magnetic tunnel junction has a soft ferromagnetic layer whose direction of magnetization is changeable, and

said inductor generates a magnetic field along an easy axis which is a direction for easy magnetization of said soft ferromagnetic layer.

10. The magnetic memory device according to claim 9, wherein

said at least one magnetic tunnel junction is provided so that said easy axis

coincides with a direction of extension of said plurality of bit lines or said plurality of word lines, and

said inductor has a coil-like shape, being so provided along the direction of extension of said plurality of bit lines or said plurality of word lines which coincides with said easy axis, as to surround said memory cell array.

11. A magnetic memory device, comprising:

at least one memory cell array consisting of

a plurality of bit lines and a plurality of word lines, intersecting one another without being in contact to make up a matrix, and

a plurality of memory cells provided at intersections of said plurality of bit lines and said plurality of word lines, including at least one magnetic tunnel junction; and

at least one flash bit line and at least one flash word line both having a flat-plate shape, being so provided outside said plurality of bit lines and said plurality of word lines in said at least one memory cell array, as to cover a formation region of said plurality of bit lines and said plurality of word lines.

12. The magnetic memory device according to claim 11, wherein

said at least one memory cell array includes a plurality of memory cell arrays,

said plurality of memory cell arrays are provided in matrix,

said at least one flash bit line and at least one flash word line include a plurality of flash bit lines and a plurality of flash word lines, respectively, which are provided in matrix along the arrangement of said plurality of memory cell arrays.

13. A magnetic memory device, comprising:

at least one semiconductor chip;

a shield body made of conductive material, for containing said at least one semiconductor chip;

a package made of resin, for containing said shield body;

a bottom-surface substrate for closing an opening of said package to seal said package;

a signal transmitting bump provided in an outer main surface of said bottom-surface substrate, for transmitting a signal between said at least one semiconductor chip and the outside; and

a shielding bump so provided as to surround said signal transmitting bump, being electrically connected to said shield body,

wherein said at least one semiconductor chip includes

a magnetic memory chip comprising a memory cell array which has a plurality of memory cells including at least one magnetic tunnel junction.

14. The magnetic memory device according to claim 13, further comprising:

a first stress relieving film provided inside and outside an opening edge of said shield body; and

a second stress relieving film provided on an inner wall of said shield body.

15. The magnetic memory device according to claim 14, wherein

said at least one semiconductor chip further includes

a circuit chip including peripheral circuits of said memory cell array, and

said magnetic memory chip and said circuit chip are contained in said shield body, being vertically layered.

16. The magnetic memory device according to claim 13, wherein

said at least one magnetic tunnel junction has a soft ferromagnetic layer whose direction of magnetization is changeable, and

said shield body is made of ferromagnetic material having magnetic permeability equal to or higher than that of said soft ferromagnetic layer.

17. The magnetic memory device according to claim 13, wherein

said shield body is made of antiferromagnetic material.

18. The magnetic memory device according to claim 13, wherein

said shield body is made of multilayer film consisting of ferromagnetic material <136a> and antiferromagnetic material.